We Claim:

1. A method for fabricating trench capacitors for memory cells having at least one selection transistor for integrated semiconductor memories, which comprises the steps of:

providing a semiconductor substrate of a first conductivity type;

producing a horizontal mask on the semiconductor substrate, the horizontal mask to be used for producing trenches;

carrying out an anisotropic etching step after a completion of the horizontal mask, thereby producing upper trench regions in the semiconductor substrate;

covering sidewalls of the upper trench regions with vertical masks;

etching the semiconductor substrate selectively with respect to the horizontal mask and the vertical masks, for producing lower trench regions;

doping surfaces of the lower trench regions with a material of a second conductivity type resulting in first electrodes being produced on surfaces of the lower trench regions;

applying a dielectric to the first electrodes;

removing the vertical masks;

applying second electrodes to the dielectric resulting in the trench capacitors being formed in the lower trench regions;

etching the semiconductor substrate in the upper trench regions after an application of the second electrodes;

producing an insulator on a region etched in each of the upper trench regions; and

producing electrically conductive connections each connecting a respective one of the second electrodes to a respective selection transistor.

2. The method according to claim 1, which further comprises forming the semiconductor substrate from one of silicon and p-doped silicon.

3. The method according to claim 1, which further comprises producing the horizontal mask as a layer stack using a photolithographic process.

4. The method according to claim 3, which further comprises forming the layer stack to have at least one of a nitride layer and an oxide layer.

5. The method according to claim 1, which further comprises affecting the anisotropic etching of the semiconductor substrate using a dry etching process.

6. The method according to claim 1, which further comprises forming the upper trench regions in each case to project into the semiconductor substrate to a depth of about 500 nm to 1500 nm.

7. The method according to claim 1, which further comprises producing the vertical masks by conformally depositing a

covering layer and subsequent anisotropic etching the covering layer.

8. The method according to claim 7, which further comprises forming the covering layer from at least one material selected from the group consisting of nitrides and oxides.

9. The method according to claim 1, which further comprises producing the lower trench regions by anisotropic etching.

10. The method according to claim 9, which further comprises enlarging a surface of the lower trench regions by isotropic etching.

11. The method according to claim 1, which further comprises forming the trenches to have a depth of about 5 µm to 15 µm.

12. The method according to claim 1, which further comprises enlarging a surface of the lower trench regions by producing mesopores in a manner subsequent to the etching of the lower trench regions.

13. The method according to claim 1, wherein the doping of the lower trench regions connects the first electrodes of adjacent trenches to one another in a low-impedance manner.

14. The method according to claim 1, wherein the dielectric completely covers the first electrodes in the lower trench regions.

15. The method according to claim 1, which further comprises forming the dielectric as a layer selected from the group consisting of an oxide-nitride-oxide layer, a nitride-oxide layer, an oxide layer, an Al_2O_3 layer, a Ta_2O_5 layer, a hafnium oxide layer, a layer containing Al_2O_3, and a combination of these layers.

16. The method according to claim 15, which further comprises converting the nitride-oxide layer into an oxide layer in the upper trench regions.

17. The method according to claim 1, which further comprises producing the second electrodes by filling the trenches with a conductive material as far as the upper trench regions.

18. The method according to claim 17, which further comprises using doped polysilicon as the conductive material for forming the second electrodes.

19. The method according to claim 1, which further comprises replacing the vertical masks with the insulators having a low dielectric constant after a production of the second electrodes.

20. The method according to claim 19, which further comprises forming the insulators from silicon oxide.

21. The method according to claim 19, which further comprises forming the insulators with a predetermined layer thickness.

22. The method according to claim 1, which further comprises electrically conductively connecting each of the second electrodes of the trench capacitors to a diffusion location of the respective selection transistor.

23. The method according to claim 1, which further comprises removing the horizontal mask.

24. The method according to claim 1, which further comprises removing the vertical masks before applying the dielectric.

25. The method according to claim 1, which further comprises removing the dielectric in the upper trench regions.

26. The method according to claim 1, which further comprises producing the insulators on the semiconductor substrate in the upper trench regions after removing the vertical masks.

27. The method according to claim 1, which further comprises:

forming a liner in the upper trench regions; and

etching selectively the semiconductor substrate with respect to the liner in the upper trench regions after applying the second electrodes.

28. The method according to claim 1, which further comprises during the etching in the upper trench regions,

opening the semiconductor substrate with an aid of double etching-back of the second electrodes.

29. The method according to claim 1, which further comprises performing the following steps after an application of the dielectric:

filling the trenches with a material forming the second electrodes;

etching-back the material forming the second electrodes as far as a first etching-back step within the upper trench regions;

covering trench walls above the first etching-back step with a liner;

etching-back the material forming the second electrodes as far as a second etching-back step; and

opening the semiconductor substrate selectively with respect to the liner.

30. The method according claim 27, which further comprises

applying the liner to one of the dielectric and the semiconductor substrate.

31. The method according to claim 27, which further comprises:

applying the liner to the dielectric; and

converting the liner into an oxide.